UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,331	02/20/2002	Ruban Kanapathippillai	42P14039	9807

8791 7590 08/26/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,331	KANAPATHIPPILLAI ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 - 28 have been examined. Claims 1 - 28 have been rejected.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are informal. Formal drawings are required. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On page 17, line 18, Figure 2B is referenced. It appears that the reference should be to Figure 3B.

Claim Objections

4. Claim 11 is objected to because of the following informalities: Claim 11 recites, "a serial test port to access the debug registers serially". It appears that "to access the debug registers serially" could either mean, "to access the debug registers in sequence one after the other" or "to access the debug registers using a serial access method to send and receive data." For the purpose of claim examination, the phrase, "a serial test port to access the debug registers serially" is interpreted as "a serial test port to access the debug registers using a serial access method to send and receive data."
5. Claim 22 is objected to because of the following informalities: Claim 22 recites, "a serial test port to load the debug registers serially". It appears that "to load the debug registers serially" could either mean, "to load the debug registers in sequence one after the other" or "to load the debug registers using a serial access method to send and receive data." For the purpose of claim examination, the phrase, "a serial test port to load the debug registers serially" is interpreted as "a serial test port to load the debug registers using a serial access method to send and receive data."
6. Claim 22 is objected to because of the following informalities: The claim refers to "a integrated circuit test system" rather than "an integrated circuit test system." Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7.1. Claims 1, 8 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims recite, "parallel I/O mapped debug access". The term "I/O mapped" does not appear to be a term in the art. For the purpose of claim examination, the phrase, "parallel I/O mapped debug access" is interpreted as "parallel I/O memory mapped debug access". Correction or amendment is required.

7.2. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites a debug instruction "PRAM." The Examiner cannot determine what function the PRAM instruction performs. The specification appears to indicate that PRAM is a feature, as opposed to an instruction. For the purpose of claim examination, the phrase, "PRAM" is interpreted as "the feature parameter RAM". Correction or amendment is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann (U.S. Patent Number 6,041,406) in view of Edwards (U.S. Patent 6,591,369).

9.1. **Regarding claim 1**, Mann teaches:

9.1.1. selecting one or more access methods (**column 12, lines 45 - 48**) provided in an integrated circuit to debug program code and/or circuitry contained therein (**Abstract, lines 1 - 2**), the access methods including,

9.1.2. a serial debug access through a serial I/O test port of the integrated circuit (**Abstract, lines 1 - 5**),

9.1.3. a parallel direct debug access through I/O pads of the integrated circuit **(figure 2, elements 214 with attached signal definitions, 208, 210; and column 13, lines 42 - 67; and column 14, lines 18 - 26)**.

9.2. **Regarding claim 1**, Mann does not specifically teach:

9.2.1. selecting one or more ***of three*** access methods provided in an integrated circuit to debug program code and/or circuitry contained therein, the ***three*** access methods including,

9.2.2. a parallel I/O mapped debug access through a host I/O port of the integrated circuit

9.3. **Regarding claim 1**, Edwards teaches:

9.3.1. selecting one or more access methods provided in an integrated circuit to debug program code and/or circuitry contained therein **(Abstract, lines 8 - 10)**.

9.3.2. a parallel I/O mapped debug access through a host I/O port of the integrated circuit **(column 3, lines 17 - 20; and figure 1; and column 7, lines 57 - 63; and column 8, lines 4 - 7; and column 7, lines 49 - 57; and figure 3, especially element 106, 305, 311a, 311b, 303; and column 10, lines 1 - 5)**.

9.4. The motivation to use the art of Edwards with the art of Mann would have been the benefit recited in Edwards that a high-speed link is provide by the invention to allow real-time collection of trace information, including all information that an external system would use for debugging a processor **(column 2, lines 56 - 62)**.

9.5. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use common knowledge in the art with the art of Mann to produce the claimed invention.

9.6. **Regarding claim 2**, Edwards teaches:

9.6.1. setting a test mode input on an I/O pad of the integrated circuit **(column 18, lines 7 - 9, i.e. TMS signal)**.

9.7. **Regarding claim 3**, Mann teaches:

9.7.1. the parallel direct debug access is through host I/O pads around circuitry of the host I/O port **(figure 2, elements 214, 210)**.

9.8. **Regarding claim 4**, Edwards teaches:

9.8.1. debugging the integrated circuit using test/debug instructions and data **(figure 4, element 401; and column 10, lines 41 - 67)**.

9.9. **Regarding claim 5**, Mann teaches:

9.9.1. the debugging of the integrated circuit includes setting a plurality of registers in the integrated circuit to control the debugging of the integrated circuit **(column 3, lines 29 - 37)**.

9.10. **Regarding claim 7**, Mann teaches:

9.10.1. the serial debug access method is selected and the setting of the plurality of registers is serially performed (**figure 2, elements 204, TDI, 212, 210; column 5, lines 37 - 65**).

9.11. **Regarding claim 8**, Edwards teaches:

9.11.1. the parallel I/O mapped debug access method is selected and the setting of the plurality of registers is performed in parallel by memory map addressing of the plurality of registers and the data therein (**column 3, lines 17 - 20; and figure 1; and column 7, lines 57 - 63; and column 8, lines 4 - 7; and column 7, lines 49 - 57; and figure 3, especially element 106, 305, 311a, 311b, 303; and column 10, lines 1 - 5**).

9.12. **Regarding claim 9**, Mann teaches:

9.12.1. the parallel direct debug access method is selected and the setting of the plurality of registers is performed in parallel directly addressing each of the plurality of registers and the data therein (**figure 2, elements 214 with attached signal definitions, 208, 210; and column 13, lines 42 - 67; and column 14, lines 18 - 26**).

9.13. **Regarding claim 11**, Mann teaches:

9.13.1. An integrated circuit (**Abstract**);

9.13.2. debug registers to control on-chip testing and debugging of the integrated circuit (**figure 2, element 210; and column 5, lines 44 - 50**);

9.13.3. a serial test port to access the debug registers serially (**Abstract, lines 1 - 5; and figure 2, elements 204 (with signals TDI, TDO), 212, 210; and column 3, lines 29 - 34**);

9.13.4. I/O pads to access the debug registers in parallel using direct access (**figure 2, elements 214 with attached signal definitions, 208, 210; and column 13, lines 42 - 67; and column 14, lines 18 - 26**).

9.14. **Regarding claim 11**, Mann does not specifically teach:

9.14.1. a host I/O port to access the debug registers in parallel using I/O memory mapped access (**figure 2, elements 104, 202, 208, 210, 218, 200; and column 3, lines 31 - 35; and column 24, lines 55 - 57**); and

9.15. **Regarding claim 11**, Edwards teaches:

9.15.1. a host I/O port to access the debug registers in parallel using I/O memory mapped access (**column 3, lines 17 - 20; and figure 1; and column 7, lines 57 - 63; and column 8, lines 4 - 7; and column 7, lines 49 - 57; and figure 3, especially element 106, 305, 311a, 311b, 303; and column 10, lines 1 - 5**).

9.16. The motivation to use the art of Edwards with the art of Mann would have been the benefit recited in Edwards that a high-speed link is provide by the invention to allow real-time collection of trace

information, including all information that an external system would use for debugging a processor (column 2, lines 56 - 62).

9.17. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards with the art of Mann to produce the claimed invention.

9.18. **Regarding claim 17**, Mann teaches:

9.18.1. one or more functional blocks having circuitry to test and debug (figure 2, element 104).

9.19. **Regarding claim 18**, Edwards teaches:

9.19.1. one or more memories having program code to test and debug (figure 2, elements 102, 105, 201; and column 8, lines 45 - 55; and column 13, lines 14 - 22; these recited passages obviously require program code in memory that is being tested).

9.20. **Regarding claim 19**, Edwards teaches:

9.20.1. a global memory having program code to test and debug (figure 2, elements 102, 105, 201; and column 8, lines 45 - 55; and column 13, lines 14 - 22; these recited passages obviously require program code in memory that is being tested).

9.21. **Regarding claim 22**, Mann teaches:

9.21.1. A integrated circuit test system (figure 1; and column 4, lines 22 - 50).

9.21.2. an integrated circuit (Abstract, lines 1 - 2) including,

9.21.2.1. debug registers to control on-chip testing and debugging of the integrated circuit (figure 2, element 210; and column 5, lines 44 - 50),

9.21.2.2. a serial test port to load the debug registers serially (Abstract, lines 1 - 5; and figure 2, elements 204 (with signals TDI, TDO), 212, 210; and column 3, lines 29 - 34),

9.21.2.3. I/O pads to load the debug registers in parallel using direct access (figure 2, elements 214 with attached signal definitions, 208, 210; and column 13, lines 42 - 67; and column 14, lines 18 - 26); and

9.21.3. a tester (figure 1, elements H and 112) including,

9.21.3.1. a processor readable storage medium (figure 1, element 112), and

9.21.3.2. code recorded in the processor readable storage medium (figure 1, element 112),

9.21.3.2.1. to test and debug the integrated circuit (figure 1, element 112),

9.21.3.2.2. to interface the tester to the serial test port of the integrated circuit to load the debug registers serially (column 25, lines 15 - 22; and column 3, lines 29 - 34),

9.21.3.2.3. to interface the tester to the I/O pads of the integrated circuit to load the debug registers in parallel using direct access (column 25, lines 15 - 22; and column 3, lines 29 - 34; and column 24, lines 55 - 57).

9.22. **Regarding claim 22**, Mann does not specifically teach:

9.22.1.1. a host I/O port to load the debug registers in parallel using I/O memory mapped access, and

9.22.1.2. to interface a tester to the host I/O port of the integrated circuit to load the debug registers in parallel using I/O memory mapped access

9.23. **Regarding claim 22**, Edwards teaches:

9.23.1. a host I/O port to load the debug registers in parallel using I/O memory mapped access **(column 3, lines 17 - 20; and figure 1; and column 7, lines 57 - 63; and column 8, lines 4 - 7; and column 7, lines 49 - 57; and figure 3, especially element 106, 305, 311a, 311b, 303; and column 10, lines 1 - 5)**.

9.23.2. to interface the tester to the host I/O port of the integrated circuit to load the debug registers in parallel using I/O memory mapped access (figure 1, especially elements 103, 107, 106; and **column 3, lines 17 - 20; and figure 1; and column 7, lines 57 - 63; and column 8, lines 4 - 7; and column 7, lines 49 - 57; and figure 3, especially element 106, 305, 311a, 311b, 303; and column 10, lines 1 - 5)**.

9.24. The motivation to use the art of Edwards with the art of Mann would have been the benefit recited in Edwards that a high-speed link is provide by the invention to allow real-time collection of trace information, including all information that an external system would use for debugging a processor **(column 2, lines 56 - 62)**.

9.25. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Edwards with the art of Mann to produce the claimed invention.

9.26. **Regarding claim 23**, Edwards teaches:

9.26.1. The integrated circuit test system of claim 22, wherein the processor readable storage medium is one or more of the set of magnetic storage medium, optical storage medium, or semiconductor storage medium **(figure 1, element 112)**.

10. **Claims 6, 20, and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann in view of Edwards as applied to claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above, and further in view of Mann729 (U.S. Patent 6,094,729).

10.1. **Regarding claim 6**, Mann as modified by Edwards teaches the access methods and methods of selecting the access method, and debugging, as recited in claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above.

10.2. **Regarding claim 6**, Mann729 teaches:

10.2.1. the plurality of registers in the integrated circuit control a debug controller in the integrated circuit to control the debugging **(figure 2, elements 210, 218, 208; and column 5, lines 43 - 49)**.

10.3. **Regarding claims 20 and 21**, Mann as modified by Edwards teaches the integrated circuit as recited in claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above.

10.4. **Regarding claim 20**, Mann and Edwards does not specifically teach:

10.4.1. a debug controller coupled to the debug registers, the debug controller to test and debug circuitry within the integrated circuit in response to the information stored in the debug registers

10.5. **Regarding claim 20**, Mann729 teaches:

10.5.1. a debug controller coupled to the debug registers, the debug controller to test and debug circuitry within the integrated circuit in response to the information stored in the debug registers **(figure 2, elements 210, 218, 208; and column 5, lines 43 - 49)**.

10.6. The motivation to use the art of Mann729 with the art of Mann would have been the benefits recited in Mann729 that the debug interface and associated operation method has many advantages, including compact trace formats that efficiently store important operational information in a limited storage space **(column 3, lines 35 - 42)**.

10.7. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mann729 with the art of Mann to produce the claimed invention.

10.8. **Regarding claim 21**, Mann teaches:

10.8.1. the information stored in the debug registers is one or more debug instructions of the set of break execution, inject command, single step **(column 16, lines 14 - 33; and table 7, command code 0111, subcode 2, instruction step)**, reset, break at address, and PRAM.

11. **Claims 10, 12 - 15 and 24 - 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann in view of Edwards as applied to claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above, and further in view of common knowledge in the art.

11.1. **Regarding claim 10**, Mann as modified by Edwards teaches the access methods and methods of selecting the access method, and setting a test mode, as recited in claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above.

11.2. **Regarding claim 10**, Mann and Edwards does not specifically teach:

11.2.1. the setting of the test mode input controls a select input control of a multiplexer in the integrated circuit to select between parallel I/O mapped debug access and parallel direct debug access to debug the integrated circuit.

11.3. **Regarding claims 12 - 15**, Mann as modified by Edwards teaches the integrated circuit, as recited in claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above.

11.4. **Regarding claims 24 and 25**, Mann as modified by Edwards teaches the integrated circuit test system, as recited in claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above.

11.5. **Regarding claims 12 and 24**, Mann and Edwards does not specifically teach:

11.5.1. a multiplexer to select between loading the debug registers in parallel with the host I/O port and the I/O pads.

11.6. **Regarding claims 13 and 25**, Mann and Edwards does not specifically teach:

11.6.1. the multiplexer is responsive to a test mode input of an I/O pad.

11.7. **Regarding claims 13 and 25**, Edwards teaches:

11.7.1. setting a test mode input on an I/O pad of the integrated circuit **(column 18, lines 7 - 9, i.e. TMS signal)**.

11.8. **Regarding claims 10, 12, 13, 24 and 25**, Official Notice is taken that it was common knowledge in the art at the time of invention to set a select input control of a multiplexer in order to route one of a plurality of multiplexer input signals to the multiplexer output. The motivation would have been to avoid duplicating circuit components by using common components to process either signal.

11.9. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use common knowledge in the art with the art of Mann and Edwards to produce the claimed inventions.

11.10. **Regarding claim 14**, Mann does not specifically teach:

11.10.1. a demultiplexer to select between reading information from the debug registers in parallel with the host I/O port and the I/O pads.

11.11. **Regarding claim 15**, Mann does not specifically teach:

11.11.1. the demultiplexer is responsive to a test mode input of an I/O pad.

11.12. **Regarding claim 15**, Edwards teaches:

11.12.1. setting a test mode input on an I/O pad of the integrated circuit **(column 18, lines 7 - 9, i.e. TMS signal)**.

11.13. **Regarding claims 14 and 15**, Official Notice is taken that it was common knowledge in the art at the time of invention to set a select control of a demultiplexer in order to route a signal to one of a plurality of demultiplexer output signals. The motivation would have been to avoid duplicating circuit components, such as debug registers, by using common components to process either signal.

11.14. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use common knowledge in the art with the art of Mann and Edwards to produce the claimed inventions.

12. **Claims 16 and 26 - 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mann in view of Edwards as applied to claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above, and further in view of Swoboda (U.S. Patent 6,754,599).

12.1. **Regarding claim 16,** Mann as modified by Edwards teaches the integrated circuit system as recited in claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above.

12.2. **Regarding claim 16,** Mann and Edwards does not specifically teach:

12.2.1. one or more digital signal processing units to test and debug.

12.3. **Regarding claim 16,** Swoboda teaches:

12.3.1. one or more digital signal processing units to test and debug **(figure 2, element 140; and column 16, lines 25 - 30).**

12.4. **Regarding claims 26 - 28,** Mann as modified by Edwards teaches the integrated circuit test system as recited in claims **1 - 5, 7 - 9, 11, 17 - 19 and 22 - 23** above.

12.5. **Regarding claim 26,** Mann and Edwards does not specifically teach:

12.5.1. the integrated circuit is a packaged integrated circuit and the tester is a packaged integrated circuit tester to test and debug the packaged integrated circuit.

12.6. **Regarding claim 26,** Swoboda teaches:

12.6.1. the integrated circuit is a packaged integrated circuit and the tester is a packaged integrated circuit tester to test and debug the packaged integrated circuit **(figure 2; and column 3, line 61 through column 5, line 67).**

12.7. **Regarding claim 27,** Mann and Edwards does not specifically teach:

12.7.1. the integrated circuit is packaged and coupled to a printed circuit board and the tester is a printed circuit board tester to test and debug the printed circuit board including the integrated circuit.

12.8. **Regarding claim 27,** Swoboda teaches:

12.8.1. the integrated circuit is packaged and coupled to a printed circuit board and the tester is a printed circuit board tester to test and debug the printed circuit board including the integrated circuit **(figure 2; and column 3, line 61 through column 5, line 67).**

12.9. **Regarding claim 28,** Mann and Edwards does not specifically teach:

12.9.1. the integrated circuit is packaged and coupled to a printed circuit board which is inserted into a system and the tester is a system tester to test and debug the system and the printed circuit board including the integrated circuit.

12.10. **Regarding claim 28,** Swoboda teaches:

12.10.1. the integrated circuit is packaged and coupled to a printed circuit board which is inserted into a system and the tester is a system tester to test and debug the system and the printed circuit board including the integrated circuit (**figure 2; and column 3, line 61 through column 5, line 67**).

12.11. The motivation to use the art of Swoboda with the art of Mann and Edwards would have been the benefit recited in Swoboda that the invention was an integrated circuit constructed for easy debug and emulation (**column 6, lines 1 - 5**).

12.12. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Swoboda with the art of Mann and Edwards to produce the claimed inventions.

Conclusion

13. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.
14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.
15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.
16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul L. Rodriguez 8/22/05

Primary Examiner
Art Unit 2125

RG